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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,772	01/08/2002	Keum-Nam Kim	1514.1006	6312

21171 7590 07/13/2004

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,772	KIM, KEUM-NAM	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group II, claims 7-22 in the reply filed on 6/4/04 is acknowledged. The traversal is on the grounds that there have been no references cited to show any necessity for requiring restriction, and that the evaluation of both sets of claims would not provide an undue burden upon the examiner in comparison with the additional expense and delay to Applicants in filing a divisional. This is not found persuasive because the product as claimed could be made by another and materially different process, such as forming opening portions by selective deposition of the insulating layers or by masking with a material other than photoresist, rather than following the methodology recited in claims 7-22, thus making the product and process claims distinct inventions. Additionally, since any prior art meeting the limitations of the product claims may not meet the limitations of the method claims, the examiner would be required to separately consider and search the distinct process and product limitations when considering patentability. Thus, consideration of the two distinct groups would present a serious burden to the examiner. Since the inventions are distinct, are classified in different classes, and would require different searches or consideration of prior art, the requirement is still deemed proper and is therefore made FINAL.

2. Claims 1-6 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 6/4/04.

Claim Objections

3. .Applicant is advised that should claim 10 be found allowable, claim 12 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 7, 9, 10-15, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,087,730 to McGarvey et al.

Regarding claim 7, McGarvey discloses: forming a pixel electrode (20) and a semiconductor layer (50) spaced apart from each other on a substrate (30; figures 1-3); forming an first insulating layer (38) over a surface of the substrate to cover the pixel electrode and the semiconductor layer (column 10, lines 46-50; it is implicit that the layer covers the pixel electrode, since it is blanket deposited on the substrate (also see figure 3; layer 38 partially covers the pixel electrode); forming a gate electrode (37) on a portion of the first insulating layer corresponding to a location of the semiconductor layer (figures 1, 3; column 10, lines 46-55); forming a second insulating layer (54) to cover the gate electrode (figures 1, 5); forming a

photoresist layer over the surface of the substrate, exposing a portion of the second layer over the pixel electrode, and etching the first and second insulating layers to form an opening portion using the photoresist as a mask (figures 1 and 5; see column 10, line 65 – column 11, line 6 and column 8, lines 33-50), this set of procedures including forming contact holes in the insulating layers to expose portions of the pixel electrode and semiconductor layer; and forming source and drain electrodes in the contact holes, the source electrode connected to the semiconductor layer and the drain electrode connecting the semiconductor layer and pixel electrode (see figure 1; column 10, line 65 – column 11, line 6; column 8, lines 33-50; McGarvey teaches usage of photolithographic masking and etching to form contact holes for metal traces 39 and 40; since contacts are touching the pixel electrode and semiconductor portions, they are considered to be 'exposed' or present under an "opening portion").

Regarding claim 9, McGarvey discloses forming the pixel electrode before forming the semiconductor layer (figures 4B, 4C, 5).

Regarding claims 10 and 12, McGarvey discloses forming a polysilicon layer on the substrate; and patterning the polysilicon layer to form the semiconductor layer (figure 4C, 5; column 10, lines 11-45).

Regarding claim 11, McGarvey discloses depositing an amorphous silicon layer on the substrate (column 10, lines 10-15); annealing the amorphous silicon layer to form a polysilicon layer (column 10, lines 40-45); and patterning the polysilicon layer to form the semiconductor layer (column 10, lines 35-45).

Regarding claim 13, McGarvey discloses depositing a first metal layer (155) on the first insulating layer (figures 1 and 5), and patterning the first metal layer to form the gate electrode (figures 1, 3, 5).

Regarding claim 14, McGarvey discloses forming source (51) and drain (52) regions at the end of the semiconductor layer (figure 1).

Regarding claim 15, McGarvey discloses depositing a second metal layer (39, 40) on the second insulating layer (figures 1, 5), and patterning to form source and drain electrodes (figures 1 and 5 show that the layer is clearly patterned).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 19, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over McGarvey et al. in view of U.S. Patent No. 6,480,577 to Izumi et al.

McGarvey discloses forming the second insulating layer, masking with photoresist, and then removing the photoresist (see figure 1; column 10, line 65 – column 11, line 6; column 8, lines 33-50), but fails to disclose forming a third insulating layer before etching the opening portions.

Izumi discloses forming a third insulating layer (9) comprising an acryl layer (column 11, lines 15-20) over the device (figure 2) before forming the opening portions (figure 2; hence before forming the photoresist layer used to mask the opening portions).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the TFT of McGarvey, such that a third insulating layer comprising an acryl is formed before masking and etching the openings, as suggested by Izumi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use an acryl layer between the second insulating layer and the masking photoresist layer, because doing so helps flatten out differences in surface height over the device formation areas (see Izumi, column 11, lines 7-15), which improves the deposition, uniformity, and photolithographic patterning of all overlying layers, as is appreciated by one skilled in the art. Further, an acryl layer helps increase the distance and decrease the effective dielectric constant between wiring components provided in the device, which in turn decreases the capacitive coupling between neighboring wiring lines (see Izumi, column 6, lines 40-46).

8. Claims 16, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over McGarvey et al. in view of U.S. Patent No. 5,010,027 to Possin et al.

Regarding claims 16 and 21, McGarvey fails to disclose that forming the opening portion comprises using the photoresist as a planarization layer.

Possin discloses a flat panel display in which a photoresist planarization layer is deposited on top of the structure, and used in an opening formation process (see column 2, lines 25-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of McGarvey to use a photoresist layer as a planarization layer during the opening formation step, as suggested by Possin. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a photoresist planarization layer, because doing so allows for greater accuracy in forming opening portions, which in turn improves the device performance or allows for greater miniaturization (see Possin, column 1, lines 12-35; column 2, lines 25-46). It is generally known in the art, and thus well within the purview of a person skilled in the art, that performing photolithographic methodology on a planarized surface produces more precise results than performing such steps on a non-planar surface.

Regarding claim 18, McGarvey discloses that the pixel electrode is formed before forming the semiconductor layer (figures 4B, 4C, 5).

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over McGarvey et al. in view of U.S. Patent No. 6,346,978 to Hsu et al.

McGarvey fails to teach that the pixel electrode can be formed after forming the semiconductor layer.

Hsu teaches forming the semiconductor layer (figure 5), and then forming the pixel electrode (figure 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method steps of McGarvey, such that the silicon layer is formed before the metal layer, as suggested by Hsu. The rationale is as follows: A person having ordinary skill

in the art would have been motivated to provide the silicon layer first, because doing so allows the silicon layer to be annealed at very high temperatures, thus providing a substantially single crystal SOI layer for improved TFT performance. (see Hsu, column 3, lines 35-55). A person skilled in the art would recognize that it is advantageous to provide the silicon layer first, because the pixel electrode materials cannot withstand the anneal temperatures required to produce single crystal silicon (see Hsu, column 3, lines 35-55; McGarvey; column 3, lines 30-60).

10. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over McGarvey et al. in view of Possin et al., as applied to claim 16, supra, and further in view of Hsu et al.

McGarvey fails to teach that the pixel electrode can be formed after forming the semiconductor layer.

Hsu teaches forming the semiconductor layer (figure 5), and then forming the pixel electrode (figure 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method steps of McGarvey as modified by Possin, such that the silicon layer is formed before the metal layer, as suggested by Hsu. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide the silicon layer first, because doing so allows the silicon layer to be annealed at very high temperatures, thus providing a substantially single crystal SOI layer for improved TFT performance. (see Hsu, column 3, lines 35-55). A person skilled in the art would recognize that it is advantageous to provide the silicon layer first, because the pixel electrode materials cannot withstand the anneal

temperatures required to produce single crystal silicon (see Hsu, column 3, lines 35-55; McGarvey; column 3, lines 30-60).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,897,328 to Yamauchi et al. and U.S. Patent No. 6,111,619 to He et al. disclose alternate methods for a flat panel display having a pixel electrode and a channel region of a top-gate TFT formed laterally spaced apart at the same level above the substrate.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Carl Whitehead Jr.
CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd